

# HP E1437A

## **Technical Specifications**



**HP E1437A** 

Whether you analyze spectra or capture waveforms, the HP E1437A ADC will help you see signal features you may have never seen before.

## A Remarkable Digitizer

At the heart of the HP E1437A is an exceptionally low distortion digitizer. Low distortion means high quality data will reveal even more about your signal when averaged, filtered or FFT processed.

## Analog Signal Conditioning

You aren't restricted to operating the HP E1437A at a specific amplitude operating point thanks to built-in analog signal conditioning.

#### **Digital Filtering and LO**

Use the 24 real-time digital filters built-in to the HP E1437A to increase the precision of the output samples, or filter out extraneous signals.

## **FIFO Memory**

The FIFO means you won't lose new samples while you are transferring a data block out.

## VXI*plug&play* programming

The HP E1437A is VXI*plug&play* compatible and is shipped with software and documentation to support a broad set of controllers, and operating systems.

# 20 MSample/second ADC with Filter and FIFO

Rev. June 1997

#### **High Speed Data Transfers**

VXI Local Bus capability means HP E1437A can output data at 40 MB/s continuously and as high as 60 MB/s when transferring blocks of data.

## **Specification Note**

Specifications describe warranted performance over the temperature range of 0° to 55° C, after a 15-minute warm-up from ambient conditions and automatic calibrations enabled unless otherwise noted. Supplemental characteristics identified as "typical" or "characteristic," provide useful information by giving non-warranted performance parameters. Typical performance is applicable from 20° to 30° C.

## Abbreviations

 $\label{eq:matrix} \boldsymbol{dBm} = dB \text{ relative to 1 mW into} \\ 50 \boldsymbol{\Omega}$ 

**dBfs** = dB relative to full scale amplitude range.

 $\mathbf{dBc} = \mathbf{dB}$  relative to carrier amplitude.

Typical = typical, non-warranted, performance specification included to provide general product information.

Input Modes	DC coupled, AC coupled. Input grounded, input co Input BNC shell grounded	
Full Scale Input Ranges	Volts peak	dBm, 50 ${f \Omega}$
(ADC clipping levels, dBm values are approximate )	10.24 V 5.12 V 2.56 V 1.28 V 640 mV 320 mV 160 mV 80 mV 40 mV 20 mV	30 24 18 12 6 0 - 6 - 12 - 18 - 24
Maximum Input Level		
(for any time interval > 10 ms)	10 Vrms for 5.12 and 10. 5 Vrms for all other range	
Return loss of 50 $\Omega$ input impedance		
(± 1%, DC coupled, BNC shell grounded, frequency < 8MHz)	> 40 dB	
AC Coupling Characterisitics		
(A 0.2 $\mu\text{F}$ capacitor is placed in series with the input signal)	0.2 µF (typical) Maximum DC voltage is	± 50 V
Common Mode Characteristics		
Shell floating impedance Shell grounded impedance Maximum Current (diode clamped to < ± 1 V peak)	50 <b>Ω</b> in parallel with 0.0 < 0.1 <b>Ω</b> (typical) ± 1 amp peak	4 μF (typical)
Common Mode Response	Range	Response in dBfs
(Response to a sine wave voltage source of amplitude Vcom (in mV) applied through a 50 $\Omega$ serie resistor; frequency < 8 MHz.)	30 dBm to 0 dBm s — 6 dBm — 12 dBm to — 24 dBm	<pre>&lt; ( - 90 +20 × LOG(Vcom)) &lt; ( - 80 +20 × LOG(Vcom)) &lt; ( - 65 +20 × LOG(Vcom))</pre>

Input

Accuracy

Resolution	
Raw ADC resolution	23 bits, two's complement
After digital zoom and filter operations	32 bits, full resolution mode 16 bits, reduced resolution mode
Amplitude Accurracy: (< 100 kHz, 25 °C, analog alias	s filter on, digital decimation filters off, DC coupled)
Absolute voltage measurement accuracy 12 dBm range	± 0.03 dB
Range accuracy relative to 12 dBm range	$\pm$ 0.03 dB (for all ranges)
Alias filter off relative to alias filter on mode at 12 kHz	± 0.02 dB
Temperature drift	< 0.001 dB/°C (typical) of deviation from 25°C
DC offset	
Temperature drift	
30 dBm to – 6dBm ranges – 12 to – 24 dBm ranges	< ± 0.01%/°C (typical) < ± 0.1 mV/°C (typical)
Input bias current (in parallel with 50 $oldsymbol{\Omega}$ input load)	< 64 µA
Flatness (dB peak-to-peak, excluding digital filter respor	ise)
Alias filter on	
freq < 100 kHz	< 0.03 dBpp
freq < 5 MHz	< 0.25 dBpp
freq < 8 MHz	< 0.80 dBpp
Alias filter off	
freq < 8 MHz	< 0.25 dBpp
freq < 40 MHz	3 dBpp (typical)
Anti-alias filter stopband rejection (12 MHz to 20 MHz)	> 100 dB

#### Dynamic Range

**NOTE:** The performance specifications for the spurious response and discrete sidebands characteristics require that the mainframe containing the HP E1437A have Option 918 (connector shields E1400-80920) installed. In addition all modules in the mainframe must comply with the VXI 1.4 specification for ECL trigger lines; and the 10-MHz VXI system clock must be turned off. External clock input must be disconnected when not being used for ADC clock.

#### Signal to Noise Ratio

The reference signal is a sine wave with peaks at the clipping voltage of the current range; typical values)

Alias	filter	on

— 6 dBm to 30dBm ranges	71 dB
— 12 dBm range	70 dB
— 18 dBm range	68 dB
— 24 dBm range	65 dB
Alias filter off	
— 6 dBm to 30dBm ranges	68 dB
— 12 dBm range	66 dB
— 18 dBm range	61 dB
— 24 dBm range	57 dB

#### Input Noise Density (Alias filter on, Internal sample clock)

– 6 dBm to 30dBm ranges 1 MHz to 8 MHz 100 kHz to 1 MHz 10 kHz to 100 kHz 1 kHz to 100 kHz 10 Hz to 1 kHz	– 140 dBfs/Hz – 138 dBfs/Hz – 135 dBfs/Hz – 131 dBfs/Hz – 101 – 10* LOG (f) dBfs/Hz	
<ul> <li>12 dBm range</li> <li>1 MHz to 8 MHz</li> <li>100 kHz to 1 MHz</li> <li>10 kHz to 100 kHz</li> <li>1 kHz to 100 kHz</li> <li>1 kHz to 10 kHz</li> <li>10 Hz to 1 kHz</li> </ul>	– 139 dBfs/Hz – 137 dBfs/Hz – 134 dBfs/Hz – 129 dBfs/Hz – 99 – 10*LOG(f) dBfs/Hz	— 151 dBm/Hz — 149 dBm/Hz — 146 dBm/Hz — 141 dBm/Hz — 111 — 10*LOG(f) dBm/Hz
- 18 dBm range 1 MHz to 8 MHz 100 kHz to 1 MHz 10 kHz to 100 kHz 1 kHz to 10 kHz 10 Hz to 1 kHz	– 137 dBfs/Hz – 135 dBfs/Hz – 131 dBfs/Hz – 125 dBfs/Hz – 95 – 10*LOG(f) dBfs/Hz	— 155 dBm/Hz — 153 dBm/Hz — 149 dBm/Hz — 143 dBm/Hz — 113 — 10*LOG(f) dBm/Hz
— 24 dBm range 1 MHz to 8 MHz 100 kHz to 1 MHz 10 kHz to 100 kHz 1 kHz to 100 kHz 10 Hz to 1 kHz	– 134 dBfs/Hz – 132 dBfs/Hz – 127 dBfs/Hz – 120 dBfs/Hz – 90 – 10*LOG(f) dBfs/Hz	— 158 dBm/Hz — 156 dBm/Hz — 151 dBm/Hz — 144 dBm/Hz — 114 — 10*LOG(f) dBm/Hz

<b>Spurious Response</b> (2 kHz to 8 MHz, termir	nated with 50 Ohm, input B	NC shell grounded)
DSP clock = ADC clock, alias filter on DSP clock ≠ ADC clock, alias filter on DSP clock = ADC clock, alias filter off		
Phase Noise		
Phase noise density (Single sideband power density of a 5 MHz signal, vibration < 0.05G)		
Δf = 100 kHz Δf = 1 kHz Δf = 100 Hz	20 MHz clock <	20.48 MHz clock < 138 dBc/Hz < 130 dBc/Hz < 120 dBc/Hz
Discrete sidebands (100 Hz < ∆f < 1 MHz, other modules must comply with VXI 1.4 specification for ECL trigger lines, External Clock disconnected)		
Internal clock	<— 100 dBc	
Internal clock (distributed on backplane with CLK10 backplane clock disabled)	<-80 dBc(typical)	
Distortion		
Harmonic distortion products to 8 MHz	< — 75 dBc a	r < — 110 dBfs

(Includes aliased distortion components)	
Intermodulation Distortion products to 8 MHz (two tones each at — 6 dBc)	<-75 dBc or <-110 dBfs

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Clock

<b>Clock Input/Output Characteristics</b> External ADC clock input (AC coupled with small-signal input impedance of 100 kΩ above 10 kHz. Large signals are diode clamped through 100 Ω)	TTL, ECL, or > — 6 dBm sine waves, BNC input
Intermodule Synchronization Clock/SYNC	ECL-10 K compatible, SMB
Clock Source Frequencies	
Internal ADC clock	20 MHz or 20.48 MHz
External sample clock frequency range DSP clock = ADC clock DSP clock ≠ ADC clock	2 MHz to 20.60 MHz 0 Hz to 20 MHz
DSP clock Internal ADC	20 MHz or 20.48 MHz ADC clock must be > 2 MHz in this mode
Internal Clock Characteristics	
Frequency Accuracy (20 MHz or 20.48 MHz, 0°C to 40°C)	±100 Hz
40°C) Jitter	< 5 ps rms (typical) (see phase noise specification for spectral content of jitter)
Sampling Skew (typical)	
Within mainframe (rear clock distribution) Between mainframes (clock extended via a 1 m coaxial cable)	< 10 ns (typical) < 25 ns (typical)

Trigger	
Trigger sources	External TTL/ECL/sine wave, level, LOG(magnitude), software (via register write)
Slope	Positive/negative
Threshold	
Level trigger	$V_{range} \times N/128$ , -128 $\leq N \leq 128$ ; hysteresis is $\frac{V_{range}}{256}$
LOG(magnitude) trigger	$V_{range}(dBm)-N\times0.3762574~dBm,0\leq N\leq255;$ hysteresis is 1.5 dB
External trigger input	TTL/ECL/Sine wave, BNC
Trigger offset	
Resolution (in output sample periods)	1 sample, 32-bit complex data 2 samples, 16-bit complex or 32-bit real data 4 samples, 16-bit real data
Maximum pre-trigger delay	$(132 - \frac{\text{dramsize}}{8}) \times \text{trigger offset resolution}$
Maximum post-trigger delay	16,777,116 $ imes$ trigger offset resolution

Trigger

Filtering

$$\mathbf{H}(f) = \mathbf{H}_{\text{analog}}(f) \cdot \mathbf{H}_{\text{digital}}\left(N, \frac{f - f_0}{f_s}\right)$$

where:

Analog frequency response function (typical), with alias filter off.

$$H_{\text{analog}} = \prod_{n=1}^{5} \frac{1}{1 - jf / B_n}$$

n	Poles, Bn (IVIHz)
1	-80.234 +j 0.0
2	-103.94 +j 0.0
3	-103.94 -j 0.0
4	-72.9774 +j 49.94437
5	-72.9774 -j 49.94437

Analog Frequency Response Function (typical), with alias filter on.

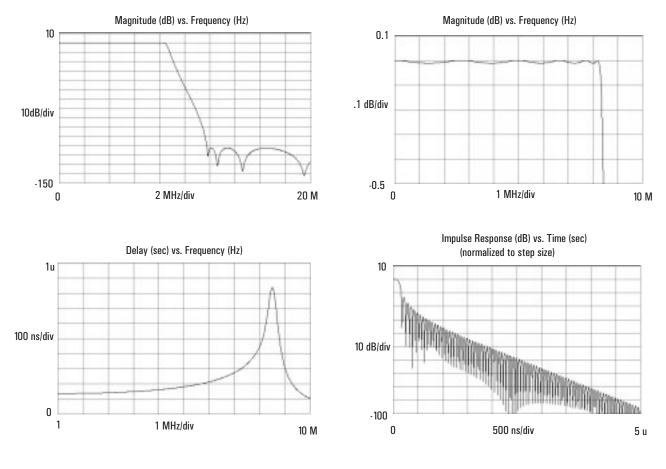
$$\mathbf{H}_{\text{analog}} = \prod_{n=1}^{11} \frac{1 - jf / A_n}{1 - jf / B_n}$$

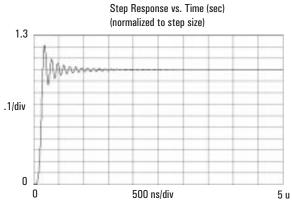
n	Zeros, An (MHz)	Poles, Bn (MHz)
1	$\infty$	-3.423881 +j 0.0
2	-0.278765 + j37.0	-3.122370 +j 3.010688
3	-0.278765 -j 37.0	-3.122370 -j 3.010688
4	-0.085700 +j 19.5	-2.397607 +j 5.453639
5	-0.085700 -j 19.5	-2.397607 -j 5.453639
6	-0.053075 +j 14.6	-1.579759 +j 7.117287
7	-0.053075 -j 14.6	-1.579759 -j 7.117287
8	-0.042453 +j 12.6	-0.864515 +j 8.088296
9	-0.042453 +j 12.6	-0.864515 +j 8.088296
10	-0.038826 +j 11.84	-0.271817 +j 8.524792
11	-0.038826 -j 11.84	-0.271817 -j 8.524792

Digital Frequency response function

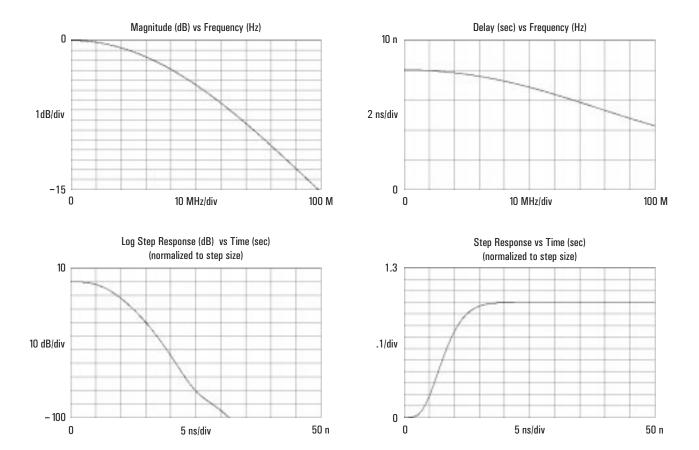
$$H_{digital}\left(N, \frac{f-f_0}{f_s}\right) = \begin{bmatrix} 1, N=0\\\\\prod_{n=1}^{N} \left(\frac{z^3 + 2z^2 + 2z + 1}{4z^3 + 2z}\right)^5 \\\\ z = e^{j2^n p \left(f-f_0\right)/f_s}, N > 0 \end{bmatrix}$$

## Filter characteristics for nominal analog alias filter, N = 0

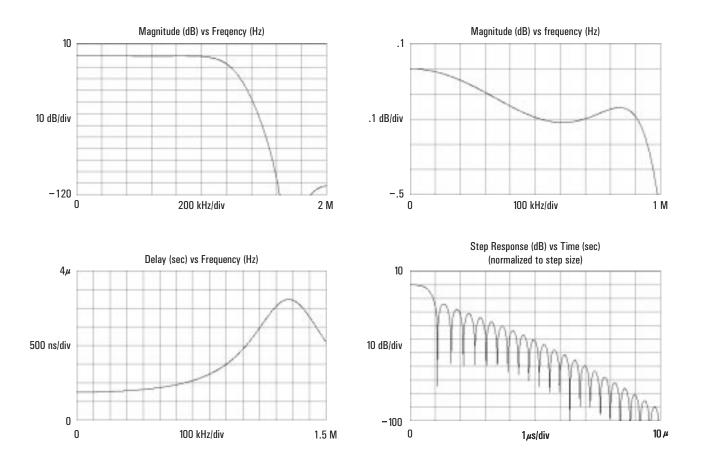


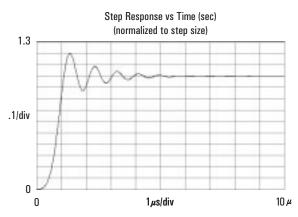


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 $12 \ {\rm of} \ 16$ 

Programming (all functions are programmable via the VXI register interface)

Center frequency	
Resolution	ADC clock frequency $\div$ (1024 $\times$ 10 <sup>9</sup> )
Range	$\pm$ ADC clock frequency ÷ 2
Filtering and decimation	
Bandwidths ( — 15 dB) (See the frequency response section for filter characteristics)	$\pm 0.5 \times Fs/2^N$ , $0 \le N \le 24$
Output sample rate	Fs/2 <sup>N</sup> (nyquist sampled) 2 × Fs/2 <sup>N</sup> (2X over-sampled)
Data output	
Туре	real, complex
Resolution	16 bits, 32 bits
Output ports	VME data transfers
	Local Bus data transfers
Transfer rate	60 MByte/s, burst
	40 MByte/s, sustained
	2 MByte/s, VME
Block sizes	8, 16, 32,, up to memory size bytes
Measurement modes	Block mode (individually triggered blocks)
	Continuous mode
Information available in read registers	
Manufacturer's code	4095 decimal (Hewlett-Packard)
Model code	534 decimal (HP E1437A)
Other Status bits	Measurement loop status, Ready, ADC error, Ext clk
	error, Set-up error, Sync/Idle complete,
	Read Valid, Measure done, Armed, FIFO overflow,
	Overload, Error, Mod ID, Hardware set.
Interrupts	Two independent priority interrupts initiated by
	masked status bits
Memory	
Туре	FIFO
Capacity	8 MBytes (4 MSamples, 16 bits)
	16 MBytes (8 MSamples, 16 bits) option UFC
	32 MBytes (16 MSamples, 16 bits) option ANC
	64 MBytes (32 MSamples, 16 bits) option ANE

VXI Standard Information	Conforms to VXI Rev. 1.4 C-size, single slot width Register/Message based programming "Slave" Data Transfer Bus functionality A16 address capability D16 data capability Local Bus capability Requires ECLTRG0 and ECLTRG1 lines for module synchronization	
Size (single slot, C-size VXI module)		
Dimensions	14 inches deep, 9.2 inches high, 1.2 inches wide (approx 36 cm deep, 23 cm high, 3 cm wide)	
Weight	3.9 pounds (approx 1.8 kg)	
Software Drivers		
Driver Type	C libraries with source code	
Supported Operating Systems	Windows 3.1®, Windows95, WindowsNT™, HP-UX* 9.X	
Supply Media	Disk, DAT	

\*HP-UX 9 X and 10.0 for HP 9000 Series 700 and 800 computers are X/Open Company UNIX 93 branded products

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## Regulatory Compliance

Safety Standards	Designed for compliance to CSA C22.2, No. 231 Designed for compliance to UL 1244, 4th Edition Designed for compliance to IEC 348, 2nd Edition, 1	
Radiated Emisions	CISPR 11 :1990 Group 1, Class A (requires connector shield's E1400-80920 in the mainframe)	
Environmental		
Operating Restrictions Ambient Temperature	0° to 55°C	
Humidity, Non-condensing Maximum Altitude	10% to 90% at 40°C 4600 m (15,000 ft) Above 2285 m (7500 ft), derate operating temperature by — 3.6°C per 1000 m ( — 1.1°C per 1000 ft)	

Storage and Transport Restrictions

Ambient Temperature Humidity, Non-condensing Maximum Altitude — 40° to 70°C max 95 % RH at 65°C 4600 m (15,000 ft)



#### **General Characteristics**

#### VXI Power Requirements

•		
Range	DC Current	Dynamic Current
+ 5 V	5.0 A	0.50 A
-5.2 V	5.0 A	0.50 A
- 2 V	0.3 A	0.10 A
+ 12 V	1.0 A	0.050 A
- 12 V	1.2 A	0.050 A
+ 24 V	0 A	0 A
- 24 V	0 A	0 A
2 4 9		

#### VXI Cooling Requirements

15° C rise

Calibration interval

Warm up time

15 minutes

1 year

4.0 liters/second 0.5 mm H<sub>2</sub>0

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